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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/528,035	12/16/2005	Juergen Einspenner	I431.125.101/FIN 249 PCT/	9035

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
07/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/528,035	EINSPENNER ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-37* is/are pending in the application.

4a) Of the above claim(s) *14-22 and 29-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/16/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is response to Election Restriction filed on 06/19/2007. Claims 14-37 are pending; Claims 23-28 are elected for the exam; and Claims 14-22 and 29-37 are withdrawing without traverse.

However, Applicant(s) is required to cancel the non-elected claims in the next communication.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. PCT/DE03/03208, filed on 03/16/2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 23-28 are rejected under 35 U.S.C. 102(e) as being anticipated by (US Patent 6,773,960) (hereinafter as '960)(see entire document).

5. With respect to claim 23, Fee discloses a method for determining the arrangement of contact areas ('960, figs. 1-5, element [34]) on an active top side (active top surface) ('960, figs. 1-5, element [22]) of a semiconductor chip (semiconductor die

or device) ('960, figs. 1-5, element [20]) arranged in or on a housing (slot in a die attach or die-receiving area) ('960, figs. 1-5, element [14]) ('960, the abstract, col. 1, ll. 12-25), the method being performed on a computer system, comprising:

reading semiconductor chip (semiconductor die or device) ('960, figs. 1-2, element, [20]) data into the computer system, the semiconductor chip data comprising geometrical properties of the semiconductor chip and information about a number of contact areas to be arranged at each edge of the semiconductor chip ('960, col. 5, ll. 1-14, col. 7, line 60 – col. 8, line 6);

reading contact area ('960, figs. 1-5, element [34]) data into the computer system, the contact area data comprising geometrical and electrical properties of contact areas to be arranged on the active top side of the semiconductor chip ('960, col. 5, ll. 55-65 and col. 6, ll. 8-17);

reading housing (slot in a die attach or die-receiving area) ('960, figs. 1-5, element [14]) data into the computer system, the housing data comprising geometrical and electrical properties of the housing and also of contact pads arranged on a top side of the housing ('960, col. 5, line 66 – col. 6 line 17 and col. 6, ll. 27-48);

reading production (assemblies) data into the computer system, the production data defining the arrangement of the semiconductor chip in relation to the housing ('960, col. 5, line 66 – col. 6 line 17, col. 8, line 50 – col. 9, line 10);

generating a model of an electronic device ('960, figs. 1-5), which comprises the housing and the semiconductor chip arranged with its passive rear side (backside) ('960, figs. 1-5, element [33]) on the top side (top surface) of the housing, from the

semiconductor chip data, contact area data, housing data and production data ('960, col. 3, ll. 48-60, col. 4, ll. 16-31, and col. 7, line 60 – col. 8, line 23);

arranging the contact areas in the model of the electronic device in edge regions on the active top side of the semiconductor chip ('960, figs. 1-5, element [34], col. 3, ll. 32-47, col. 5, line 55 – col. 6, line 7); and

providing the contact area arrangement data for subsequent fabrication and/or design processes of the semiconductor chip (semiconductor die) and/or of the housing (slot in a die attach or die-receiving area) and/or of the electronic device ('960, col. 3, line 60 – col. 4, lien 5, and col. 6, ll. 32-40).

6. With respect to claim 24, Fee discloses the method of claim 23, comprising arranging the contact areas in such a way that the contact areas ('960, figs. 1-5, element [34]) in each case lie on straight connecting lines (conductive element) ('960, figs 1-5, element [43]) between the contact pads (bond pad) ('960, figs. 1-5, element [12]) within the housing and the area centroid of the active top side of the semiconductor chip ('960, col. 5, ll. 55-65, col. 6, ll. 8-17, figs. 1-5 with descriptions).

7. With respect to claim 25, Fee discloses the method of claim 23, comprising wherein in the case of contact areas arranged at a respective semiconductor chip edge, distances of identical magnitude in each case are provided between adjacent contact areas and/or between the respective outermost contact areas per semiconductor chip edge and the adjoining semiconductor chip edges ('960, col. 5, ll. 28-50, col. 6, ll. 8-17, figs. 1-5 with descriptions).

8. With respect to claim 26, Fee discloses the method of claim 23, comprising wherein the contact areas are firstly in each case arranged on connecting lines between the contact pads on the top side of the housing and the area centroid of the active top side of the semiconductor chip ('960, col. 5, ll. 55-65, col. 6, ll. 8-17, figs. 1-5 with descriptions).

9. With respect to claim 27, Fee discloses the method of claim 23, comprising wherein the contact areas arranged at an identical semiconductor chip edge are subsequently displaced such that the distances between adjacent contact areas and/or between the respective outermost contact areas per semiconductor chip edge and the adjoining semiconductor chip edges are formed with the same magnitude in each case ('960, col. 5, ll. 28-50, col. 6, ll. 8-17, figs. 1-5 with descriptions).

10. With respect to claim 28, Fee discloses the method of claim 23, comprising wherein the distances between the contact areas and contact pads that are to be electrically connected to one another in each case are minimized ('960, col. 5, ll. 55-65, col. 6, ll. 8-17, figs. 1-5 with descriptions).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nghia M. Doan
Patent Examiner
AU 2825
NMD

7/17/2007

THUAN V. DO
PRIMARY PATENT EXAMINER